REMARKS

Claims 2-12 and 18 are pending in this application. By this Amendment, claims 2 and 12 are amended. Applicants submit that these amendments do not introduce new matter, as support may be found, among other places, at pages 45-47 and 63-65 of the specification.

In the Action, claims 12 and 18 stand rejected under 35 U.S.C. §102(b) as being anticipated by *Park et al.* (U.S. Pat. No. 5,521,115). Claims 2 and 6-10 stand rejected under 35 U.S.C. §103(a) as being obvious over *Park et al.* in combination with *Lu* (U.S. Pat. No. 5,843,820). Claim 11 stands rejected under 35 U.S.C. §103(a) as being unpatentable over a three-way combination of *Park et al.*, *Lu*, and *Bronner et al.* (U.S. Pat. No. 5,606,188). Claims 3-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over a three-way combination of *Park et al.*, *Lu*, and *Ishii.* (U.S. Pat. No. 5,250,831). Applicants respectfully traverse these grounds of rejection, especially should they be applied to the pending claims as amended.

Amended independent claim 2 recites, among other features, the following features:

> "an element isolation insulating film buried in said semiconductor layer to define a plurality of active element areas each spreading over two adjacent trench capacitors;
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> a plurality of transistors formed two by two in each of said plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of said source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors, said transistors each having a gate connected to a word line continuous in one direction, each of said trenches of two adjacent trench capacitors is located under the gate of a corresponding transistor;"

The novel device recited in claim 2 offers an improved memory device having advantageous characteristics, such as a higher density of capacitors due to its novel arrangement.

In rejecting claim 2, the Action primarily relies on *Park et al.* Action, pp. 3-4. The Action admits, however, that *Park et al.* fails to show the recited feature of "the other of said

source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors." Action, p. 4. In an effort to overcome this admitted deficiency in *Park et al.*, the Action alleges that *Lu* teaches this missing feature, and that it would have been obvious to one of ordinary skill to incorporate this alleged *Lu* feature in the *Park et al.* device. Applicants respectfully disagree.

The Action's proposed combination would destroy the *Lu* device, obviating any benefits achieved from the *Lu* invention. *Lu* relates generally to a horizontal trench capacitor having a small height-to-width aspect ratio. See *Lu*, col. 1, lines 18-19 and Fig. 12, element 50. The patent makes clear that its disclosed invention benefits from having such shallow, wide capacitors, and expressly distinguishes these capacitors from prior art deep trench capacitors. *Lu*, col. 3, lines 55-59 ("The improved DRAM cell structure takes advantage of forming the capacitors with increased horizontal dimensions in the substrate to increase the capacitance without having to etch exceptionally deep trenches with high aspect ratios (depth/width), as formed by the conventional method.") (emphasis added). The width of the *Lu* horizontal capacitor provides the key feature to its invention: an amorphous silicon layer 54' formed above the capacitor that starts out wide near the capacitor's anode 50, and then gradually becomes narrow towards the upper surface of the device. *See Lu*, Fig. 9 (dashed lines); and col. 8, lines 31-40 (describing this as the invention's "key feature"). *Lu* relies on the width of the horizontal capacitor to allow this tapering to occur.

In sharp contrast, *Park et al.* uses the very type of deep trench capacitor that *Lu* avoids. *Park et al.* expressly states that "[i]n a manner similar to the prior art, a storage capacitor is formed in a deep trench 22 adjacent to the storage node 20 . . ." *Park et al.*, col. 5, lines 8-10 (emphasis added). Indeed, *Park et al.* expressly recites the depth of the trench when claiming its own disclosed invention. See, e.g., *Park et al.*, claim 1 (". . . each trench penetrating into said substrate and substantially into said buried region;") (emphasis added). One of ordinary skill,

reading the teachings of *Lu* and *Park et al.*, would not be led to make the combination proposed in the Action. To the contrary, one of ordinary skill would see that *Park et al.* uses deep trench structures, that *Lu* avoids them, and would recognize that the two inventions should not be combined as suggested in the Action.

To further illustrate this point, Applicants note that the claim 2 device recites "a plurality of transistors formed two by two in each of said plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of said source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors." The *Lu* area, defined by STIs 12, is only shown as having a single transistor 16, and only a single capacitor. See, e.g., *Lu,* Fig. 12. Indeed, the preferred width of the *Lu* horizontal capacitor appears to occupy nearly the entire area between STIs 12, and there simply is not room in there for more than one transistor and more than one capacitor. See, e.g., *Lu* Figs. 11-12. If the *Lu* device were incorporated in the *Park et al.* device, the result would still not render the claim 2 device obvious, as there would only be a single transistor and a single capacitor in the area between STIs.

Claim 2 has also been amended to recite "each of said trenches of two adjacent trench capacitors is located under the gate of a corresponding transistor." Neither *Park et al.* nor *Lu*, alone or in combination, discloses such a feature. Regarding *Park et al.*, the trenches 22 are not located under the gate of a corresponding transistor. See, e.g., *Park et al.* Fig. 3 (forming trench 22) and 10 (showing transistors). Regarding *Lu*, it does not disclose "two adjacent trench capacitors" at all. See, e.g., *Lu* Figs. 1-12. The resulting combination, even assuming it could be

made, would have just a single *Lu* horizontal trench capacitor and single transistor, as shown in *Lu* Fig. 12[1].

Applicants respectfully submit that amended independent claim 2 distinguishes over the applied references, and is in condition for allowance. Claims 3-11 depend from claim 2, and are allowable for at least the same reasons as claim 2, and further in view of the various advantageous and novel features recited therein. For example, dependent claim 7 recites the following:

> The semiconductor memory device according to claim 2, wherein:
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> said semiconductor layer comprises a first epitaxially grown layer and a second epitaxially grown layer formed on said first epitaxially grown layer;
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> said contact layer is formed such that said contact layer is buried in said first epitaxially grown layer to reach said capacitor node layer; and
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> the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer.

The action cites *Park et al.* strap 26 to show the claimed contact layer, and node 20 to show the claimed "other of said source/drain diffusion layers." Action, p. 4. Claim 7 recites that the "other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer." Looking at *Park et al.*, no such feature is shown. Applying the Action's interpretation of *Park et al.*, node 20 simply does not have a bottom surface connected to a top surface of strap 26. See *Park et al.*, Fig. 10. Claim 10 also recites, among other features, "the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said

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[1] Applicants have also amended claim 2 to recite additional features regarding the second contact layer to recite a revised desired invention.

contact layer." Additionally, claim 9 recites, among other features, "the other of said source/drain diffusion layers is connected to a top surface of said contact layer through a connection conductor formed on a surface thereof." The *Park et al.* node 20 does not meet these requirements.

Amended independent claim 12 recites, among other features, "an element isolation insulating film including a first insulating film buried to define active element areas inside said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film, said second insulating film buried inside said semiconductor substrate and positioned over the first insulating film." The novel device recited in claim 12 also provides an improved semiconductor memory.

In rejecting claim 12, the Action relies entirely on *Park et al.*, alleging that every recited feature is taught by this patent. With regard to the first and second insulating films recited above, the Action alleges that the *Park et al.* layer 56 shows the claimed first insulating film, and that the *Park et al.* layer 80 shows the claimed second insulating film. Action, p. 3. As amended, claim 12 recites the "first insulating film buried to define active element areas inside said semiconductor substrate." *Park et al.* layer 56 is not part of the substrate 10, but is rather deposited upon substrate 10. *Park et al.*, col. 7, lines 20-21. This layer 56 is not, however, "buried to define active element areas inside said semiconductor substrate," as recited in amended claim 12. Furthermore, claim 12 recites a "second insulating film buried inside said semiconductor substrate and positioned over the first insulating film." *Park et al.* layer 80, like layer 56, is also not part of the substrate 10, but is rather deposited upon substrate 10. *Park et al.*, col. 8, lines 56-57. As such, the *Park et al.* layer 80 is not "buried inside said semiconductor substrate and positioned over the first insulating film," as recited, among other features, in amended claim 12.

Applicants submit that amended claim 12 distinguishes over the art of record, and is in condition for allowance. Claim 18 depends from claim 12, and is allowable for at least the same reasons as claim 12, and further in view of the various advantageous and novel features recited therein.

For at least the foregoing reasons, it is respectfully submitted that the pending claims 2-12 and 18 are in condition for allowance. Should the Examiner believe that further discussion and/or amendment would be helpful to place the application in condition for allowance, the Examiner is invited to telephone the Applicants' undersigned representative at the number appearing below.

Respectfully submitted,

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